

Description

Polycrystalline Silicon Layer With Nano-grain Structure and Method of Manufacture

BACKGROUND OF INVENTION

[0001] TECHNICAL FIELD

[0002] The field of the invention is that of integrated circuit fabrication, in particular forming very small structures from polycrystalline silicon.

[0003] Current CMOS scaling trends require the poly gate length to become smaller with successive generations of technology. Currently, state of the art high performance logic uses gates that are well below 100nm, and more preferably below 30nm. On the other hand, standard poly Si grains sizes are approximately 40–70nm. This implies that the grain size of poly Si is approaching the same dimensions as the physical dimension as the gate itself.

[0004] Another important feature of CMOS scaling is electrical

thinning of the gate oxide. One disadvantage of using poly-Si as the gate conductor is that the poly-Si becomes depleted in the region of the SiO₂-poly-Si interface as a result of channel inversion. The unwanted depletion is an effective electrical thickening of the gate oxide. Improving gate activation minimizes poly depletion effects. Therefore, it would be desirable to improve poly Si gate activation.

[0005] The standard approach in the art has been that small poly crystals are best produced by maintaining the temperature of the wafer being coated at a temperature close to and only slightly above the crystallization temperature of silicon. In the case of some tools, we can monitor only substrate holder temperature. Below that temperature, the silicon film is amorphous. The standard reference book on silicon processing technology, Silicon Processing for the VLSI Era, by S. Wolf and R.N. Tauber, Volume I – Process Technology (Publisher Lattice Press, Sunset Beach, California, 1986) teaches this low temperature approach, which does produce smaller grains than earlier methods, but not enough to be suitable for 30nm gate dimensions.

[0006] Those skilled in the art will appreciate that amorphous silicon produces a highly uniform film, but is not desirable

for use as a transistor gate and other sub-100nm processing because amorphous silicon turns into far larger grain poly-Si due to the higher temperature (higher than the amorphous-Si deposition temperature) anneals that used to occur after deposition. Since the current and future technology needs sub-50nm poly-si gate CD, larger grain poly-si makes poly-si etch and poly-si doping more difficult.

[0007] Thus, there is a need for deposition methods which will enable polysilicon films with a typical grain size of below 20 nm, and preferably below 10 nm.

SUMMARY OF INVENTION

[0008] The invention relates to a technique for depositing polycrystalline silicon with small grain sizes having a mean size of less than 30nm.

[0009] A feature of the invention is that the reactant gases are heated differently from the substrate.

[0010] Another feature of the invention is that the substrate is maintained at a temperature considerably higher than the crystallization temperature.

[0011] Another feature of the invention is the formation of a structured silicon film that has small grains of poly-si at the bottom and amorphous silicon at the top.

BRIEF DESCRIPTION OF DRAWINGS

- [0012] Figure 1 shows a schematic view of a deposition apparatus.
- [0013] Figure 2A shows a simplified view of a prior art silicon film.
- [0014] Figure 2B shows a similar simplified view of a film formed according to the invention.
- [0015] Figure 3 shows a cross section of a FET made according to the invention.

DETAILED DESCRIPTION

- [0016] Figure 1 shows a simplified representation of a deposition apparatus suitable for use with the invention, such as a single wafer tool, in which vacuum chamber 100 encloses a substrate 110 that holds wafer 115 during the deposition process.
- [0017] On the left of the Figure, gas source 150 represents the supply for the reactant gases that enter the chamber along pipe(s) 155 and combine in the chamber to form the desired film.
- [0018] Within chamber 100, heat sources 125 (lower) and 120 (upper) direct infra-red radiation at the lower and upper surfaces of the substrate. Source 120 also heats the arriv-

ing gases. Heating coil 160 represents schematically various methods of heating the reactant gases before they are released into the chamber. Optionally, the temperature of the gases may be adjusted independently of the heat lamps heating the wafer.

[0019] The teaching of the prior art was that small poly grains are best produced by supplying equal power to the upper and lower lamps and by maintaining the substrate slightly above the crystallization temperature of 550°C.

[0020] It has been found that considerably better results are obtained by supplying a greater amount of heat to the bottom lamps and by maintaining the substrate at a temperature considerably greater than the crystallization temperature for forming poly.

[0021] Problems that arise in fabricating field effect transistors in sub-100nm dimensions include poor performance caused in part by depletion of the poly at the oxide-poly interface, caused by a lower than desirable concentration of dopant at the interface.

[0022] One possible technique to improve poly depletion is to have more active dopants at the SiO₂-poly-Si interface.

[0023] Dopants arrive at the SiO₂-Poly-Si interface by two pathways. One path is diffusion in the crystal poly Si, the other

path is by diffusion along the grain boundaries. Diffusion in grain boundaries is much faster than diffusion within the crystalline silicon. Since gate dimensions are about the same size as the poly-Si grain sizes, most of the diffusion takes place within the crystalline silicon rather than the grain boundary for nominal size transistors. This means that poly depletion may be improved for nominal gates by using poly Si with smaller grain sizes.

[0024] Figure 2A shows a schematic representation of a layer of gate oxide 210 having a layer of poly deposited on it, the poly having one layer of grains 220. The poly in Figure 2A is conventional, having crystals of normal dimension of mean length about 40nm. In this example, using a length of 80nm for the gate, there is only one grain boundary 222 in the first layer of the poly. For convenience in illustration, the grains are shown as rectangles. Those skilled in the art will appreciate that the actual grain shapes will be more complicated.

[0025] After a diffusion step, there will be a concentration of dopant at the grain boundary 222 adjacent to oxide 210, since diffusion is faster along the boundaries. Subsequent annealing and other high temperature steps will spread the dopant concentration, but this irregular initial distri-

bution is a disadvantage.

[0026] Figure 2B shows a similar structure, with crystal grains having a size of 10nm. There will be considerably more grain boundaries in this case and the initial distribution of dopant will be more uniform than in the case of Figure 2A.

[0027] Despite many attempts to arrive at process conditions to achieve small grain poly-Si we have determined that conventional LPCVD techniques are not capable of producing a suitable poly Si film. Small grain poly films deposited by LPCVD were found to have voids at the SiO₂ – poly interface which cause formidable problems for the gate stack etch since the voids get transferred down to the Si substrate. In addition, the small grain LPCVD film had very rough surface topography which causes problems for lithography.

[0028] In addition to improved gate depletion characteristics, small grain poly-Si has several advantages over conventional poly-Si films for gate electrode applications in terms of lithography and etch.

[0029] We have demonstrated that by using novel process conditions according to the invention, a smooth, small grain poly Si film may be produced. The smoother film results in improved thickness uniformity. Improved thickness con-

trol results in improved lithography and etch by enhancing line width control (ACLV) and line edge roughness (LER). It will also result in improved electrical uniformity in MOSFET devices by making vertical poly-Si doping very uniform. In this disclosure, methods are described how to optimize the grain size by changing the process conditions.

[0030] It is found that the most important parameter that affects the grain size is how the reactant gases are heated in the chamber. This is in contrast to the prior art teaching which identifies the substrate temperature as the primary parameter for controlling grain size. For instance, the reference book on silicon processing technology (by S. Wolf, Silicon Processing for the VLSI Era, Volume 1 – Process Technology) teaches that polysilicon grains can be reduced by lowering substrate temperature close to the crystallization temperature of the silicon. Eventually, the film can be made amorphous by dropping the substrate temperature to below the crystallization temperature.

[0031] Unfortunately, such an approach results into either an amorphous film where the grain boundaries are absent or a conventional polysilicon film with a typical grain size of the order of 40 nm.

[0032] Since the grain size of a polysilicon film is a random function, the quantitative measure of grain size is a statistical distribution. An experimental grain size distribution can be approximated by a Normal distribution. The Normal distribution is typically characterized by the mean value of grain size and the standard deviation of grain size. Therefore, the requirement for small grain polysilicon can be specified in terms of mean grain size and standard deviation of that.

[0033] Because the state-of-the-art gate length is about 30 nm or less, there is a need for polysilicon film with a grain distribution that has the mean grain size of about 20 nm or less and the grain size standard deviation of 10 nm or less. Such collection of grains will be referred to as "nanograins".

[0034] One objective of the present disclosure is to provide a deposition method which allows for polysilicon films with ultra small grains. Another objective of the present disclosure is a patterned polycrystalline Si film with "nanograins" such that each polysilicon structure contains at least several grain boundaries connecting the bottom interface to the top portion of the film.

[0035] Yet another objective of the present disclosure is the

MOSFET gate structure which incorporates the patterned polycrystalline Si film with "nanograins".

[0036] The experiments were performed in a commercial deposition chamber. The chamber provided means to partially decouple heating of the process gas and the substrate. The chamber was equipped with two sets of heating lamps: one placed above the substrate and the other placed below the substrate. Typically, 50% of power is supplied to the lamps on the top, and 50% at the bottom. By changing the percentage of power supplied to the top and the bottom lamp, one can change the temperature to which the gas is subjected to. We discovered that, by supplying 80% of the power to the bottom, the grain sizes reduce substantially. The application of this disclosure is not limited to a particular design of the chamber. Any chamber where the substrate and the reactant gas temperatures can be independently controlled can be used.

[0037] The total quantity of power will depend on the structure of the chamber (more distant lamps will need more input power to produce the same temperature than close lamps). Thus, the following discussion refers to the allocation of the total power.

[0038] Those skilled in the art will appreciate that the main factor

influencing grain size is unexpectedly the application of more power to the substrate than to the upper surface and the use of a much higher temperature than the crystallization temperature, contrary to the teaching of the prior art.

[0039] Tables I and II summarize the data. Though the smallest grain poly was obtained at the slowest deposition rate, there seems to be no correlation between the deposition rate and grain size. In addition, the smallest grain size was obtained at the substrate temperature range of 690–710C which is far above the crystallization temperature range of 550–600C.

[0040] The grain size references of $\langle 111 \rangle$ and $\langle 221 \rangle$ are to the standard method of description according to orientation.

[0041] The grain sizes were verified by TEM. It is seen that for the 690°C process, the silicon starts as small grains, but halfway during the process, it turns into amorphous silicon (without changing the applied heating power). This observation can have significant advantages in subsequent litho steps by making the top surface of the gate conductor smoother. Since the line width control becomes very tight in 100 nm and sub-100nm technology, the smoother surface morphology is essential to guarantee

the device performance within a small variation.

[0042] This dual structured layer (amorphous structure on the top and poly structure at the bottom) poly-Si formation technique can also reduce the number of processing steps required to amorphize the top surface of poly silicon gate during the poly-Si gate doping.

[0043] This dual structured silicon layer was observed to become a single-component polycrystalline structure as the deposition temperature increases above 650°C . The higher wafer temperature enhances the rearrangement of the silicon lattice in a certain grain structure and helping the growth of crystal structure as well-described in the conventional deposition method. Even in this single poly-Si layer, a grain size change has been observed, that is, a smaller grain at the bottom of poly-Si layer (at the oxide interface) and larger grain at the top of the layer. This is thought to be mainly due to the deposition temperature related kinetics. Once the deposition temperature is high enough to keep the polycrystalline structure, the crystal growth can be maintained in a grain so the same crystal structure becomes taller and wider as the deposition goes on. However, the deposition temperature is not high enough, in other words, in between amorphous and poly-

crystalline silicon generating temperatures, the initial crystalline structure generated by slow deposition rate as crystalline islands on the oxide layer can not maintain the crystal growth any longer after some time of growth.

Eventually, it becomes an amorphous structure after a very small grain, non-columnar poly-Si growth.

[0044] This large grain poly will make dopant diffuse faster down to the small grain poly-Si interface and the smaller grain at the bottom will increase the poly-Si doping since the dopants diffusion from the grain boundary into the crystalline silicon at the interface of SiO₂ and small grain poly-Si layer. This small grain poly layer also creates longer grain boundary paths and eventually help retard the dopant diffusion compared to vertical straight grain boundaries in the conventional columnar structured poly-Si. This is definitely beneficial by suppressing gate poly dopant penetration into the channel which is a serious challenge in the extremely scaled current and future nano-scale MOS (metal-oxide-semiconductor) technology with ultra-thin gate oxide that is in the range of about 10 Angstroms.

[0045] Thus, lower dopant concentration at the top of poly-Si and higher dopant concentration at the SiO₂/poly-Si in-

terface can be obtained. This dopant profile is beneficial to improve the device performance by reducing poly-Si depletion capacitance at the bottom and by reducing polycide resistance increase which is mainly caused by the higher dopant concentration of poly-Si at the top.

[0046] The unique process conditions that have been identified are shown to produce the smallest grain sizes to our knowledge. The grain size distribution can be determined by X-ray diffraction measurement. The result of such measurement is reported in the tables below. The 710°C process gives the smallest mean grain size of about 10nm. At both 690°C and 710°C, the smallest combined grain size was for the highest percentage of power in the lower lamps.

TABLE I

Temp (°C)	690	690	690	690	690	690
Lower Power %	44	20	80	44	44	44
Grain Size <111>	10.4	13.5	14.4	10.7	10.5	11.6
Grain Size <221>	45.3	47.2	21.4	45.3	45.	49.3

TABLE II

Temp (°C)	710	710	710	710	710
Lower Power %	20	80	44	44	44
Grain Size, nm <111>	12.8	8.6	10.2	10.9	12.4
Grain Size, nm <221>	40	10.7	42	42	50

[0047] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

[0048] What is claimed is: